Amendments to the Claims:

This listing of claims will replace all prior versions and listing of claims in the application.

Listing of Claims:

1. (Previously Presented) A data synchronization detection device comprising:

means for holding a result of data identification of code-modulated reproduced data;

means for detecting occurrence of a specified bit pattern in a bit sequence resulting from data identification;

means for counting a number of occurrences of said specified bit pattern in an arbitrary bit period;

means for specifying partitions of code modulation of said reproduced data using respective coefficient values of said pattern counting means in each bit period; and

means for shifting an input bit sequence by an arbitrary amount; wherein

the data identification result held by said means for holding is input to said means for shifting and said means for shifting outputs the data identification result at every partition of said code modulation, by bit shifting in accordance with output of said means for specifying.

2. (Previously Presented) The data synchronization detection device according to claim 1, further comprising:

means for effecting pattern comparison of a front section of the bit sequence of said data identification result with a PLO_SYNC pattern that effects reproduction of clock synchronization for data reproduction; and

means for specifying a data range in the data identification result held in said means for holding from the output of the means for effecting and the output of said means for specifying partitions; wherein

said data are selectively output and input to said means for shifting in accordance with an output of said means for specifying a data range, from the data identification result held in said means for holding.

3. (Currently Amended) The data synchronization detection device according to claim 1, further comprising:

means for comparing a pattern in a rear section of the bit sequence of said data identification result with a GAP pattern that correctly reproduces the final bits of the data; and

means for specifying a data range in the data identification result held in said means for holding from the output of said means for comparing and the output of said means for specifying partitions; wherein

said data are selectively output and input to said means for shifting in accordance with an output of said means for specifying a data range, from the data identification result held in said means for holding.

4. (Previously Presented) The data synchronization detection device according to claim 1, further comprising:

means for comparing a pattern, in a data position detection pattern provided at an intermediate position of the data, of an intermediate portion of the bit sequence of the result of data identification and the data position detection pattern; and

means for specifying a data range in the data identification result held in said means for holding from the output of said means for comparing and the output of said means for specifying partitions; wherein

said data are selectively output and input to said means for shifting, in accordance with an output of said means for specifying a data range, from the data identification result held in said means for holding.

5. (Previously Presented) The data synchronization detection device according to claim 1, further comprising:

means for inputting a data quality signal that expresses a likelihood that there is an error in the identified output of the reproduced data, and that selects said data identification result used for data synchronization detection in accordance with the data quality signal.

6. (Previously Presented) The data synchronization detection device according to claim 1, further comprising:

means for inputting a data quality signal that expresses a likelihood that there is an error in the identified output of the reproduced data, and that selects said data identification result used for data position identification in accordance with the data quality signal.

7. (Previously Presented) A signal processing device comprising:

means for applying a low-pass characteristic to an input analogue signal;

means for converting the analogue signal output by said means for applying into a digital signal;

means for equalizing the output signal of said means for converting;

means for identifying data output by said means for equalizing; and

a data synchronization detection device according to claim 1 that synchronizes data detection using the identified bit sequence of said data identification result.

8. (Previously Presented) A data synchronization detection device comprising:

a memory that holds a result of data identification of code-modulated reproduced data;

a pattern comparison circuit that detects generation of a specified bit pattern in a bit sequence of the output of data identification;

a pattern counting circuit that counts a number of occurrences of said specified bit pattern in an arbitrary bit period;

a data phase determination circuit that specifies a code-modulation partition of said reproduced data by using respective coefficient values of said pattern counting circuit in each bit period; and

a bit shifting circuit that shifts an input bit sequence by an arbitrary amount; wherein

the data identification result held in said memory is input to said bit shifting circuit and said bit shifting circuit outputs a data identification result at each code modulation partition by bit shifting in accordance with information regarding said code-modulation partition that was identified by said data phase determination circuit.

9. (Previously Presented) An information recording device comprising:

a data synchronization detection device according to claim 1;

means for decoding data in accordance with a specified code-modulation phase output by said data synchronization detection device;

a plurality of means for descrambling code-demodulated data output by said means for decoding data; and

means for detecting an error in data respectively descrambled by said plurality of means for descrambling; wherein

the output data of said means for descrambling corresponding to one in which the number of errors detected by said means for detecting error is a minimum is output as the reproduced data.

10. (Previously Presented) An information recording device comprising:

a data synchronization detection device according to claim 1;

means for code-demodulating data in accordance with a specified code-modulation phase output by said data synchronization detection device;

means for detecting errors in code-demodulated data; and

means for descrambling error-corrected data; wherein

reproduction data including scrambler information is input to said data synchronization detection device, and said means for descrambling descrambles using scrambler information in the reproduction data that has been error-corrected by said means for detecting errors, and output data of said means for descrambling is output as reproduced data.

11. (Previously Presented) An information recording device comprising:

a plurality of means for scrambling data;

means for code-modulating data respectively scrambled by said means for scrambling;

means for counting a number of occurrences of a specified bit pattern in a bit sequence of the code-modulated data in an arbitrary bit period;

means for determining whether or not a position of a data code modulation codeword partition can be specified, by the count result of the number of occurrences of the specified bit pattern being a prescribed threshold value; and

means for selecting said means for scrambling that is used in accordance with a determination result of a means for determining data phase.

12. (Previously Presented) The information recording device according to claim 11 wherein information of said means for scrambling selected by said means for selecting is recorded.

13. (Currently Amended) ~~An~~ A computer readable medium on which are recorded:

a PLO_SYNC that reproduces ~~the~~ clock synchronization of reproduction of a data signal by pulling a PLL (Phase Locked Loop) in a sector in a unit memory region;

data constituting recording information;

ECC for error correction of the data; and

a GAP that reproduces the final bits of the information by identifying said data; wherein

said PLO_SYNC and said data are recorded consecutively to ~~be adjacent to~~ each other.

14. (Previously Presented) The computer readable medium according to claim 13, wherein a signal obtained by adding said PLO_SYNC and said GAP to the data constituting the recording information is recorded as a bundled sector.

15. (Previously Presented) The computer readable medium according to claim 13, wherein a signal obtained by adding said PLO_SYNC and said GAP to scrambling information when scrambling the recording information is recorded as a bundled sector.

16. (Currently Amended) A computer readable medium containing an information recording format used in recording/reproduction of information comprising:

a PLO_SYNC pattern for reproducing clock synchronization for data reproduction;

code-modulated data;

error correction information which corrects data error; and

a GAP pattern that correctly generates the final bits of the data; wherein

a bundle of information comprising said PLO_SYNC pattern, said data, said error correction information, and said GAP pattern constitutes one sector, and wherein

said PLO_SYNC and said data are recorded consecutively to ~~be adjacent to~~ each other.

17. (Previously Presented) The computer readable medium according to claim 16, wherein data scrambling information is further included in said information constituting one sector.